REMARKS

Claims 1 and 4-16 are pending in the above referenced application.

Applicant submits herewith is a "Substitute Drawing Request" which Applicant asks the Examiner to please forward to the PTO official draftsperson to have entered in place of the originally filed 5/5, Fig. 9.

Examiner referenced a Notice of References Cited (PTO-892) in the Office Action Summary, however a copy of this form was not provided. Applicant respectfully requests that the Examiner provide a copy of the PTO-892 in the next Office Action.

In addition, Examiner is advised that a response has been concurrently filed in Application No. 09/797,899 (Attorney Docket No. MI22-1643), a divisional of the instant application, to an Office Action dated June 20, 2001. The amendments, herein, to the specification and drawing are reflective of that Office Action.

Rejection under 35 U.S.C. §103(a)

Anderson in view of Bruchhaus

Claims 1, 4-9, 11, 13-15 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Anderson (US 5,390, 072) (hereinafter "Anderson") in view of Bruchhaus (WO 9744797) (hereinafter "Bruchhaus"). Applicant traverses.

Claim 1 recites, in pertinent part, "integrated circuitry comprising a capacitor comprising a first capacitor electrode, a second capacitor electrode and a high K capacitor dielectric region received therebetween; the high K

capacitor dielectric region comprising a high K substantially amorphous material layer and a high K substantially crystalline material layer, the high K substantially amorphous material and the high K substantially crystalline material constituting different chemical compositions." Claims 4-9, 11 and 13-15 depend from Claim 1.

With regard to Anderson, the Examiner admits that such does not show that the amorphous and crystalline layers can constitute materials of different chemical constitutions as recited by Applicant's claim. For this teaching, the Examiner now turns to Bruchhaus which is represented as disclosing an invention where at least two different dielectric materials are used to form a capacitor having a desired permittivity profile. Applicant again notes that permittivity is a physical property of a material at a given temperature and is directly related to dielectric constant by the relationship $K = {}^{\varepsilon}/_{\varepsilon_0}$ where K is dielectric constant and ε and ε_0 are the permittivity of the material and of free space (generally equal to 1), respectively, at any temperature.

However, Bruchhaus is analogous to Shimizu which was cited in the previous action in an analogous combination with Anderson. Bruchhaus, as was seen for Shimizu, forms a ceramic capacitor structure that does not include any integrated circuit elements. Also analogous to Shimizu, Bruchhaus is directed to providing temperature stability for such a ceramic capacitor. Applicant respectfully asserts, then, that the methods of forming the ceramic capacitors of Bruchhaus are also analogous, in pertinent part, to the methods of Shimizu, particularly with respect to the temperatures used in the forming of the several layers.

Turning to Fig. 11 of Bruchhaus, it is seen that the desired profile provided has a range of permittivities of between about 13000 to about 16000. Anderson teaches that formed at 700°C, $BaTiO_3$ has a dielectric constant of about 330 while forming the same material at 1000°C results in a film having a dielectric constant which may exceed 1000 (see, col. 3, lines 61-68). Thus Anderson shows that the higher the temperature used in the forming of a material, the higher the dielectric constant. As the permittivities of the materials disclosed by Bruchhaus are on the order of 14,500, one of ordinary skill in the art would know that Bruchhaus, like Shimizu which disclosed permittivities of only about 1500, must employ temperatures in excess of those taught by Anderson. Such temperatures almost certainly being NOT compatible with integrated circuit processing. Thus, Applicant respectfully asserts that the processing of Bruchhaus is likely to be destructive to integrated circuitry such as is provided by Anderson. While the claims of the instant invention are directed to a structure, Applicant notes that where the process needed to form a structure in one cited reference would render structures of the other cited reference ineffective for their intended purpose, such a combination CANNOT be obvious, (see, M.P.E.P. §2143.01). Certainly the temperature required to obtain the extremely high permittivities of Bruchhaus would render Anderson unsuitable for its intended purpose. Thus Applicant asserts that the instant rejection is incorrect and must be withdrawn.

In addition, as remarked in the previous response, Shimizu is non-analogous art with respect to Anderson. Bruchhaus, being directed to the

same field and to essentially the same desired result, must then, also be non-analogous art. The Examiner is referred to MPEP: 2141.01(a) which states, citing to *In re Oetiker*, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992), that "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." Bruchhaus, like Shimizu is not an analogous field of endeavor to that of Anderson and is focused on solving a problem unrelated to the problems to which Anderson is directed. Hence Applicant respectfully asserts that the instant rejection is incorrect as provided in §2141.01(a). Thus for this additional reason alone, the instant rejection should be withdrawn.

Applicant has shown that for at least the two reasons provided above, that the instant rejection of Claims 1, 4-9, 11 and 13-15 is incorrect and should be withdrawn. Such action is earnestly sought.

Claim 10 stands rejected under 35 U.S.C. §103(s) as being unpatentable over Anderson, in view of Shimizu, as applied to Claim 1 above, and further in view of Ramakrishnan (US 5,943,580). Applicant traverses.

The Examiner states, in the Response to Arguments section of the Office Action that Applicant's previous remarks with respect to the rejections of Claims 1 and 4-16 are moot in view of the newly cited art. However, the instant rejection is identical to the rejection of the previous Office Action. In view of the Examiner's substitution of Bruchhaus for Shimizu in the previous

rejection, Applicant is assuming the same substitution was intended for the instant rejection.

Claim 10 depends from Claim 1, hence Applicant's remarks with regard to Anderson and Bruchhaus above are germane to the instant rejection of Claim 10 and are incorporated herein by reference. With regard to Ramakrishnan, the Examiner presents such art only to show that the additional aspects of Claim 10 are taught in such cited art. The Examiner does not allege that Ramakrishnan, nor does Ramakrishnan in fact, provide any teaching or suggestion to remedy the deficiencies shown above in the Examiner's combination of Anderson and Bruchhaus. Therefore, without admission as to what Ramakrishnan might teach or suggest, Applicant respectfully asserts that Claim 10 is allowable at least for the same reasons as is Claim 1.

Anderson in view of Shimizu further in view of Graettinger

Claims 12 and 16 stand rejected under 35 U.S.C. §103(s) as being unpatentable over Anderson, in view of Shimizu, as applied to claim 1 above, and further in view of Graettinger (US 5,844,771). Applicant traverses.

The Examiner states, in the Response to Arguments section of the Office Action that Applicant's previous remarks with respect to the rejections of Claims 1 and 4-16 are moot in view of the newly cited art. However, the instant rejection is identical to the rejection of the previous Office Action. In view of the Examiner's substitution of Bruchhaus for Shimizu in the previous rejection, Applicant is assuming the same substitution was intended for the instant rejection.

Claims 12 and 16 depend from Claim 1, hence Applicant's remarks with regard to Anderson and Bruchhaus above are germane to the instant rejection of such claims and are incorporated herein by reference. With regard to Graettinger, the Examiner presents such art only to show that the additional aspects of Claims 12 and 16 are taught or suggested by such cited art. The Examiner does not allege that Graettinger, nor does Graettinger in fact, provide any teaching or suggestion to remedy the deficiencies shown above in the Examiner's combination of Anderson and Bruchhaus. Therefore, without admission as to what Graettinger might teach or suggest, Applicant respectfully asserts that Claims 12 and 16 are allowable at least for the same reasons as is Claim 1.

In summary, Applicant having responded to each of the rejections and objections, respectfully asserts that Claims 1 and 4-16 are in condition for allowance. Action to that effect is earnestly sought. If, however the Examiner's next action is anything other than a Notice of Allowance, the Examiner is requested to call the undersigned to schedule a telephonic interview. The undersigned is available during normal business hours, Pacific Coast Time.

Respectfully submitted,

Dated: Oct 3, 2001

By: Bernard Berman

Bernard Berman
Reg. No. 37,279

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/512,149
Filing Date ....February 23, 2000
Inventor ....Vishnu K. Agarwal
Assignee .... Micron Technology, Inc.
Group Art Unit 2814
Examiner ....M. Pizarro Crespo
Attorney's Docket No. MI22-1322
Title: Integrated Circuitry Including a Capacitor With an Amorphous and a Crystalline High K Capacitor Dielectric Region (As Amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO SEPTEMBER 6, 2001 OFFICE ACTION

The specification has been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

at line 13 of page 11

Such integrated circuitry construction and fabrication methods might be used in a number of different applications, by way of example only in the fabrication of logic or memory circuitry, such as DRAM circuitry fabrication. Fig. 9 illustrates DRAM circuitry and fabrication thereof. A wafer fragment 110 comprises a bulk monocrystalline silicon substrate 112 having a pair of field isolation regions 114. A series of four DRAM word line constructions 116, 117, 118 and 119 are formed over the illustrated substrate, and comprise gates of respective DRAM cell field effect transistors. Gate constructions 116, 117, 118 and 119 are conventional as shown, and comprise a gate dielectric layer (not shown), an overlying conductive polysilicon region, an overlying higher conductive elemental metal or silicide region, and an

insulative cap and sidewall spacers, and which are not otherwise specifically identified with numerals. In the illustrated section, word line 117 comprises a transistor access gate having associated source/drain diffusion regions 120 and 122 formed within monocrystalline silicon substrate 12. Similarly, DRAM word line 118 comprises a gate of a DRAM cell field effect transistor having an associated pair of source/drain diffusion regions 122 and 124. Such depicts two DRAM cells which share a source/drain region ~~22~~ 122 which will electrically connect with a bit line, as described subsequently. The other respective source/drain diffusion regions 120 and ~~24~~ 124 are formed in electrical connection with DRAM cell capacitor constructions 126 and 127, respectively. The illustrated example is in the fabrication of bit line-over-capacitor DRAM integrated circuitry construction, although other DRAM integrated circuitry and other integrated circuitry constructions and fabrication methods are contemplated.

at line 21 of page 13

An insulative layer 144 is formed over DRAM capacitor cell electrode layer 140. An example and preferred material is BPSG. A contact opening 146 is formed through insulative layers 144 and 128 for ultimate formation of a conductive bit contact 156. Conductive material ~~156~~ 160 is formed within the contact opening in electrical connection with DRAM capacitor cell electrode layer 140 (not shown) and within contact opening 146 in electrical connection with bit contact source/drain diffusion region 122. Conductive material ~~156~~ 160 preferably comprises a metal and/or metal compound which is/are capable of oxidizing to a non-conductive metal oxide

upon effective exposure to the conductive metal oxide of layer 140. Preferred materials include titanium, titanium nitride, and tungsten, by way of example only. Such layers are deposited and planarized back relative to insulative layer 144 as shown.

<u>at line 9 of page 14</u>

A conductive layer 165 is deposited over and in electrical connection with conductive material ~~156~~ <u>160</u>. Such is patterned to form a DRAM bit line 166 over insulative layer 144 and in electrical connection with source/drain diffusion region 122 through conductive material ~~156~~ <u>160</u>. Other devices might be formed outwardly of layer ~~168~~ <u>165</u>, followed ultimately by formation of a final passivation layer.

No claims are amended.